ABSTRACT

The present invention pertains to formation of a transistor in a manner that mitigates overlap capacitances, thereby facilitating, among other things, enhanced switching speeds. More particularly, a gate stack of the transistor is formed to include an optional layer of poly-SiGe and a layer of poly-Si, where at least one or the layers comprises carbon. The stack may also include a polysilicon seed layer that can also comprise carbon. The carbon changes the components of sidewall passivation materials and affects etch rates during an etching process, thereby facilitating isotropic etching. The changed passivation materials coupled with an enhanced sensitivity of the poly-SiGe and carbon-doped poly-SiGe layer to an etchant utilized in the etching process causes the stack to have a notched appearance. The tapered configuration of the gate stack provides little, if any, area for dopants that may migrate under the gate structure to overlap the conductive layers in the stack, and thus mitigates the opportunity for overlap capacitances to arise.